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APPLICATION NO	. FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,961	07/15/2003	Shafqat Ahmed	42P13230D	7797
8791	7590 10/23/2006		EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN			BOOTH, RICHARD A	
SEVENTH	SHIRE BOULEVARD FLOOR		ART UNIT	PAPER NUMBER
LOS ANG	ELES, CA 90025-1030		2812	
			DATE MAILED: 10/23/200	6

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
Office Action Occurrence	10/619,961	AHMED ET AL.				
Office Action Summary	Examiner	Art Unit				
	Richard A. Booth	2812				
The MAILING DATE of this communication Period for Reply	appears on the cover sheet with	h the correspondence address				
A SHORTENED STATUTORY PERIOD FOR RE WHICHEVER IS LONGER, FROM THE MAILING - Extensions of time may be available under the provisions of 37 CF after SIX (6) MONTHS from the mailing date of this communication - If NO period for reply is specified above, the maximum statutory pe - Failure to reply within the set or extended period for reply will, by st Any reply received by the Office later than three months after the mearned patent term adjustment. See 37 CFR 1.704(b).	O DATE OF THIS COMMUNIC R 1.136(a). In no event, however, may a re i. wirod will apply and will expire SIX (6) MON tatute, cause the application to become AB.	ATION. ply be timely filed THS from the mailing date of this communication ANDONED (35 U.S.C. & 133)				
Status						
1)⊠ Responsive to communication(s) filed on 2	4 July 2006					
	This action is non-final.					
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closed in accordance with the practice und			•			
Disposition of Claims	or Expurio Quayro, 1000 o.b.	11, 400 0.0. 210.				
·						
	Claim(s) <u>61-73</u> is/are pending in the application.					
	4a) Of the above claim(s) <u>66 and 67</u> is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.						
S)⊠ Claim(s) <u>61-65 and 68-73</u> is/are rejected.						
	<u> </u>					
8) Claim(s) are subject to restriction an	id/or election requirement.					
Application Papers						
9) ☐ The specification is objected to by the Exam	niner.					
10) The drawing(s) filed on is/are: a)	accepted or b)⊡ objected to b	y the Examiner.				
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the			,			
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of: 1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the papplication from the International But * See the attached detailed Office action for a	nents have been received. The sents have been received in Appriority documents have been reau (PCT Rule 17.2(a)).	plication No eceived in this National Stage				
Attachment(s) 1) Notice of References Cited (PTO-892)	A) 🗀 Intonious Si	immary (PTO-413)				
 7)		/Mail Date				
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date		ormal Patent Application				

Art Unit: 2812

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 61-62 and 70-71 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al., U.S. Patent 6,190,981.

Lin et al. shows the invention as claimed including a method comprising: forming insulating spacers 308 adjacent to sidewalls of a gate 306; forming extension regions 310 after forming the insulating spacers by ion implantation using the insulating spacers as a mask; removing the insulating spacers by etching; and forming a source and drain 314 by ion implantation, wherein the extension regions are shallower than the source and drain, and wherein the source and drain are move heavily doped than the extension regions (see figs. 3a-3f and col. 3-line 15 to col. 4-line 45).

Regarding claims 62 and 71, note that the spacer is removed using phosphoric acid which is a wet etch.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent 6,190,981.

Lin et al. is applied as above but does not expressly disclose the spacers having a thickness of 10-200 or 20-100 angstroms. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum spacer width based upon a variety of factors including the desired offset from the gate electrode and such limitation would not lend patentability to the instant application absent a showing of unexpected results.

Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent 6,190,981 in view of Hsu et al., U.S. Patent 4,927,777.

Lin et al. is applied as above but does not expressly disclose wherein said forming the insulating spacers comprises growing an insulating layer over the gate by oxidation and removing a portion of the insulating layer that is not on the sidewalls.

Hsu et al. discloses growing an insulating layer 42 over the gate by oxidation and removing a portion of the insulating layer that is not on the sidewalls (see figs. 5-7 and col. 4-line 43 to col. 5-line 9). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Lin et al. so as to form the spacers as shown by Hsu et al. because in such a way the operating characteristics of the transistor will be improved due to the lower trap density.

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Claims 64 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent 6,190,981 in view of Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology.

Lin et al. is applied as above but does not expressly disclose the spacers being formed by LPCVD at a temperature higher than seven hundred fifty Celsius.

Wolf et al. discloses forming silicon dioxide using LPCVD in a temperature range overlapping the claimed range (see last two paragraphs on page 184). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Lin et al. so as to include the deposition process of Wolf et al. because such films show excellent conformability.

Claims 65 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent 6,190,981 in view of Shields et al., U.S. Patent 6,350,696.

Lin et al. is applied as above but does not expressly disclose removing a portion of the insulating layer using a combination of a dry and wet etch.

Shields discloses forming a spacer by a combination of a dry etch and then a wet etch (see figs. 4-7 and col. 3-lines 10-65). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Lin et al. so as to form the spacers using a dry and wet etch combination as disclosed by Shields et al. because such a process will prevent damage of the silicon and gate insulating layer from the plasma etching process.

Art Unit: 2812

Response to Arguments

Applicant's arguments with respect to claims 61-65 and 68-73 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Page 6

Richard A. Booth Primary Examiner Art Unit 2812

October 15, 2006